Towards the High-Level Design of Optical Networks-on-Chip. Formalization of Opto-Electrical Interfaces

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***Abstract*— In the near future, heterogeneous Systems-on-Chip (SoC) will become the main thrust driving the evolution of integrated circuits (IC). Thanks to the benefits that they will bring (e.g. less area, elimination of inter-chip communications, which can cause transmission delays, data corruption, and interference), the entrance of multi-technologies systems on chip in IC community is expected with optimism. However, their design is still a challenge and more work is required at the technological, architectural and system level; a key issue is the design and verification of multi-domain interfaces. This paper presents a first step towards the automatic generation of opto-elctrical interfaces, the high-level formalization of the architecture and the functionality of these interfaces.**

I. INTRODUCTION

Today, systems-on-chip are growing in complexity as a result of not only a higher density of components on the same chip but also because of the heterogeneity of different integrated modules that are particular to different application domains (such as opto-elctrical systems). Many fields benefit from these new system's advantages, among them the defense, medical, electronic, and communication. Given the diversity of concepts manipulated, the global design specification and validation are extremely challenging.

The abstraction level approach (e.g. from physical level to system level and conversely) allows many forms of design and verification that promise the reduction of the time to market and cost. A multi-disciplinary cooperation between physical and system-level designers is required to achieve accurate design and facilitate the verification step that takes more and more time in the design process. Formal methodologies have been widely used as initial exploration in the processor domain to correct light errors and defects [1]. A projection of these formal methodologies can be applied for system on chip, and in particular for specific heterogeneous interfaces as optical-electrical interfaces and photonic devices.

This paper presents the result of such cooperation proposing a the formalization of electro-optical interfaces. This formalization enables abstraction of physical level proposed solutions.

This paper is organized as follows: section 2 presents the related work; section 3 provides basic concepts of optical interfaces and photonic devices as well as DEVS formalism; section 4 shows the methodology used in this work with an optical network example and section 5 gives our conclusion.

II. RELATED WORK

A novel approach for the representation of heterogeneous systems is a formal-based description where the integration is addressed as a composition of different models of computation (MoCs). These approaches propose a single main formalism to represent the models and the main concern is building interfaces between them.

In [5] the authors propose a framework of tagged signal models for comparison of various MoCs. The framework was used to compare certain features of various MoCs such as dataflow, sequential processes, and concurrent sequential processes, Petri nets, and discrete-event systems.

The usage of MoCs in abstracting functionalities of complex heterogeneous systems was presented in [4]. The author proposes a classification of the MoCs from a denotational view, the main models being: untimed MoCs, synchronous MoCs and timed MoCs.

DEVS (Discrete Event System Specifications), an abstract simulation mechanism that enables event-based, distributed simulation and allows a dynamic representation of extended systems is presented in [8]. DEVS provides atomic modules to build complex simulations and separates the modeling and the simulation. The time advances using a continuous base. The formalism is based on the theory of systems: we have a system, a time base, inputs, states, outputs, given the current state and the inputs, established functions can be used to determine the next state and the outputs. DEVS is a formal approach to build the models, using a hierarchical and modular approach and more recently it integrates object-oriented programming techniques. Several toolkits that enable modeling and simulation based on the DEVS formalism have been developed. DEVS was successfully used for prototyping and testing environment for embedded system design, urban traffic models, and

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intrusion detection systems or for depot operations modeling but it was not used for the formalization of optical components, opto-electrical interfaces or optical networks.

The existing work on the representation of heterogeneous systems applies for Optical Networks-On-Chip (ONoC) can be divided into several classes, depending on the abstraction levels. At a lower level, we find models for physical phenomena of optics using a representation through mathematical equations. At a higher abstraction level, the models describe the behavior of the photonic devices. In [2] the authors used VHDL-AMS language while in [3], in order to model the ONoC at a high abstraction level, SystemC [7], and a bottom-up approach were used. In [6] Chatoyant was used for free space optical interconnect. The tool is based on a methodology of system level architecture design.

The work presented in this paper proposes a more generic, formal representation of the functionality and architecture of the interfaces required between electrical and optical components.

III. Basic Concepts and Definitions

This section presents the basic concepts of an optical network on chip, its electro-optical and opto-electrical interfaces and the type of network used. The DEVS formalism is also introduced [8].

A. Optical Networks-on-Chip

1) Presentation: The integrated optical communication system studied in this work, also called Optical Network on Chip (ONoC) [2], is composed of three types of blocks: *i)* transmitter interface circuits (for the electro-optical conversion) *ii)* passive integrated photonic routing structure (named λ--router) and *iii)* receiver interface circuit (for the opto-electrical conversion). A ONoC is a heterogeneous structure that can be represented as a combination of passive and active optical devices as well as mixed analog/digital integrated circuits .

2) Opto-Electrical interfaces: Each ONoC requires a transmitter block which enables the electro-optical conversion (see Fig. 1(a)). This block is mainly composed of a laser for the light emission, and its driver for the modulation and polarization.

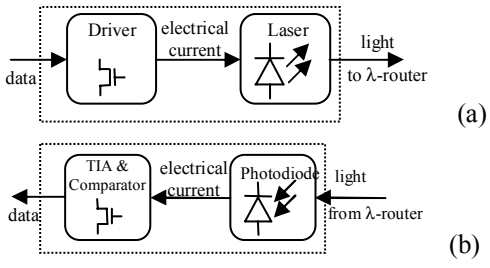

Figure 1. Transmitter (a) and receiver (b) architecture

Similar to the transmitter block, each ONoC requires a receiver block which enables the opto-electronic conversion (see Fig. 1(b)). This block is mainly composed of a photodiode (conversion of flow of photons into photocurrent), a TransImpedance Amplifier (TIA) and a decision circuit (digital signal regeneration).

B. Discrete Event System Specifications – basic notions

Discrete Event Systems Specifications (DEVS) is a formal modelling and simulation framework that supports a full range of dynamic system representation. The paradigm permits easy reuse of models that have been validated improving the security of the simulations and reducing the development time [8]. A DEVS is defined in [8] as a structure:

$DEVS = \langle X, S, Y, \delta_{int}, \delta_{ext}, \lambda, ta \rangle$ where

$X = \{(p_d, v_d) | p_d \in InPorts, v_d \in X\, p_d\}$ set of *input* ports and their values in the discrete event domain,

S - set of *sequential states*

$Y = \{(p_d, v_d) | p_d, \in OutPorts, v_d \in Y\, p_d\}$ set of *output* ports and their values in the discrete event domain.

$\delta_{int} : S \rightarrow S$ the *internal transition* function

$\delta_{ext}: Q \times X \rightarrow S$ the *external transition* function, where:

$Q = \{(s,e) | s \in S, 0 \le e \le ta(s)\}$ set of total state,

e is the *time elapsed* since the last transition

$\lambda: S \rightarrow Y$ output function

$t_a: S \rightarrow R^{+}_{0,\infty}$ set of positive reals with 0 and ∞.

The system's state is, at any time ***s.*** There are two possible situations:

1. where no internal events occur. In this case the system stays in this state ***s*** for the time $\boldsymbol{t_a(s)}$. When the elapsed time ***e*** equals $\boldsymbol{t_a(s)}$ (that is the time allocated for the system to stay in state ***s***), the system outputs the value $\boldsymbol{\lambda(s)}$ and changes to the state ***s'.*** We emphasize here that the output is possible only before the internal transitions.
2. where there is an external event ***x*** before the expiration time, ***ta(s)*** (the system is in state ***(s,e)***, with $\boldsymbol{e \le ta(s)}$), the system's state changes to state ***s'*** as a result of the transition $\boldsymbol{\delta_{ext}(s,e,x)}$.

Thus, the internal transition function dictates the system's new state when no external events occurred since the last transition while the external transition function dictates the system's new state when an external event occurs – this state is determined by the input ***x***, the current state s and how long the system has been in this state, ***e***. In both cases the system is then in some new state ***s'*** with some new expiration time ***ta(s')***.

IV. Formalization of Opto-electrical interfaces

This section presents the DEVS formalism applied to optical-electrical interfaces connecting on-chip processors and passive photonic devices. In this paper, only functional conversion interfaces are presented to prove the DEVS efficiency for the optical formalism.

A. Conversion interfaces

1) Transmitter architecture: Fig. 2 shows the DEVS optical transmitter architecture view, including the internal and external events with the Is/Os.

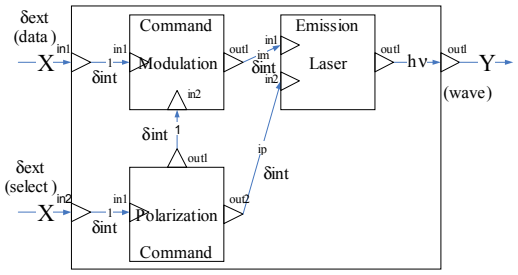

Figure 2. DEVS optical transmitter architecture view

The following equations give the formal description of the optical transmitter (electro-optical conversion) using DEVS formalism.

$$DEVS_{TX} = (X, Y, S, \delta_{ext}, \delta_{int}, \lambda, ta) \quad (1)$$

with : inputs: $InPorts = \{\text{'data'}, \text{'select'}\}$
input set: $X = \{(p,v) | p \in InPorts, v \in X_p\}$
with $X_p = \{data\_to\_send\} | \{activation\}$ and,
outputs: $OutPorts = \{\text{'wave'}\}$
output set: $Y = \{(p,v) | p \in OutPorts, v \in Y_p\}$
with $Y_p = wave\_value \in \{wavelength, power\}$

The states are : $S = \{\text{'idle'}, \text{'conversion'}\}$ (2)

The internal events are:

$\delta_{int}(phase, \sigma, local\_inport, local\_value, inport, value): S \rightarrow S$
$= (\text{'modulation'}, \sigma, p, v, latency\_mod)$ if $phase = \text{'conversion'}$ and $p = modulation\_port$ and $v = \{data\_to\_send\}$
$= (\text{'polarization'}, \sigma, p, v, latency\_pol)$ if $phase = \text{'conversion'}$ and $p = polarization\_port$ and $v = \{active\}$
or if $phase = \text{'idle'}$ and $p = polarization\_port$ and $v = \{no\_active\}$
$= (\text{'emission'}, \sigma, p, v, latency\_laser)$ if $phase = \text{'conversion'}$ and $p = laser\_port$ and $v = wave\_value$ (with *power* proportional with the modulation current I_m and the polarization current I_p of the laser driver).
$= (\text{'idle'}, \sigma, p, v)$ else.

The external events are:

$\delta_{ext}(phase, \sigma, e, x): Q \times X \rightarrow S$
$= (\text{'idle'}, e, p, v)$ if $phase = \text{'idle'}$ and $p = activation$ and $v = off$
$= (\text{'busy\_active'}, process\_time, p, v)$ if $phase = \text{'conversion'}$ and $p = activation$ and $v = on$
$= (\text{'busy\_send'}, process\_time, p, v)$ if $phase = \text{'conversion'}$ and $p = data$ and $v = data\_to\_send$
with $Q = \{(s,e) | s \in S, 0 \le e \le ta(s)\}$

Output functions are:

$\lambda(phase, \sigma, local\_inport, wave\_value, wave): S \rightarrow Y$
$= (out, wave\_value)$ if $phase = \text{'conversion'}$ and $local\_inport = laser\_port$
$= (out, 0 \cdot exp(0))$ if $phase = \text{'idle'}$

State advancing time is:

$ta(phase, \sigma): S \rightarrow \Re^{+}_{0,\infty} = \sigma = latency \mid time\_next\_data$ (3)
with $latency = latency\_mod \mid latency\_pol \mid latency\_laser$

The transmitter's behavior (as shown in (2)) is characterized by two states: *idle* (no conversion) and *conversion* (data is sent through the interface). There are 4 internal events: *modulation* (to modulate the laser with the data to convert), *polarization* (to polarize the laser), *light* (for the light emission at a given optical power and wavelength) and *idle* (no light emission); and 3 external events: *idle*, (no conversion) *selection* (conversion activation) and *data* (data to convert). The state advancing time shown in (3) is mainly composed of latencies extracted from physical design (IC) or datasheet (laser).

2) Receiver architecture: Fig. 3 shows the DEVS optical receiver architecture view, including the internal and external events with the Is/Os.

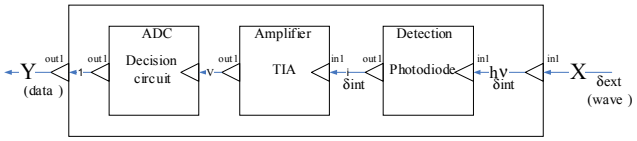

Figure 3. DEVS optical receiver architecture view

The following equations give the formal description of the optical receiver using DEVS formalism.

$$DEVS_{RX} = (X, Y, S, \delta_{ext}, \delta_{int}, \lambda, ta) \quad (4)$$

with: inputs: $InPorts = \{\text{'wave'}\}$
input set: $X = \{(p,v) | p \in InPorts, v \in X_p\}$
with $Xp = wave\_value \in \{wavelength, power\}$ and,
output: $OutPorts = \{\text{'data'}\}$
output set: $Y = \{(p,v) | p \in OutPorts, v \in Y_p\}$
with $Y_p = \{data\_to\_receive\}$

The states are: $S = \{\text{'idle'}, \text{'conversion'}\}$ (5)

The internal events are:

$\delta_{int}(phase, \sigma, local\_inport, local\_value, inport, value): S \rightarrow S$
$= (\text{'detection'}, \sigma, p, v, latancy\_pdiode)$ if $phase = \text{'conversion'}$ and $p = pdiode\_port$ and $v = wave\_value$
$= (\text{'amplifier'}, \sigma, p, v, latency\_TIA)$ if $phase = \text{'conversion'}$ and $p = TIA\_port$ and $v = photocurrent$
$= (\text{'ADC'}, \sigma, p, v, latency\_ADC)$ if $phase = \text{'conversion'}$ and $p = ADC\_port$ and $v = photocurrent \cdot gain$
$= (\text{'idle'}, \sigma, p, v)$ else.

The external events are:

$\delta_{ext}(phase, \sigma, e, x): Q \times X \rightarrow S$
$= (\text{'idle'}, e, p, v)$ if $phase = \text{'idle'}$ and $p = wave$ and $v = 0 \cdot exp(0)$
$= (\text{'busy\_receive'}, process\_time, p, v)$ if $phase = \text{'conversion'}$ and $p = wave$ and $v = wave\_value$
with $Q = \{(s,e) | s \in S, 0 \le e \le ta(s)\}$

The output functions are:

$\lambda(phase, \sigma, local\_inport): S \rightarrow Y$
$= (out, data\_to\_receive)$ if $phase = \text{'conversion'}$ and $data\_to\_receive = bit\_value$ and $local\_inport = ADC\_port$
$= (out, \text{'X'})$ if $phase = \text{'idle'}$

State advancing time is:

$ta(phase, \sigma): S \rightarrow \Re^{+}_{0,\infty} = \sigma = latency$ (6)
with $latency = latency\_pdiode \mid latency\_TIA \mid latency\_ADC$

The two states (that characterize the receiver's behavior) were taken into as shown in (5): *idle* (no conversion) and *conversion* (data is detected through the interface). However, the behavior of the receiver is easier than the receiver. There are 4 internal events: *photoconversion* (for the light conversion in photocurrent), *amplify* (for the amplification of the current and the conversion in voltage), *CAN* (for the

analog-to-digital conversion) and *idle* (no light to detect); and 2 external events: *idle*, (no conversion) and *data* (light to convert). The state advancing time shown in (6) is mainly composed of latencies extracted from physical design (IC) or datasheet (photodiode).

B. *Point to point optical connection.*

This section shows the formalization of a bidirectional point to point optical connection (fig. 4) using DEVS. A point to point connection can be a straight optical waveguide or a curve for example.

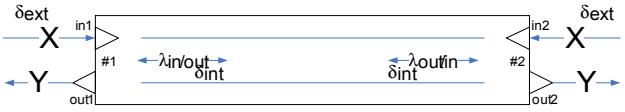

Figure 4. DEVS point to point bidirectional optical connection view

Figure 5.

$$DEVS_{P2P} = (X, Y, S, \delta_{int}, \lambda, ta) \quad (7)$$

with: inputs: $InPorts = \{\text{'in1'}, \text{'in2'}\}$

input set: $X = \{(p,v) | p \in InPorts, v \in X_p\}$

with: $X_p = wave\_value \in \{wavelength, power\}$ and,

output: $OutPorts = \{\text{'out1'}, \text{'out2'}\}$

output set: $Y = \{(p,v) | p \in OutPorts, v \in Y_p\}$

with: $Y_p = wave\_value \in \{wavelength, power\}$

The states are: $S = \{\text{'idle'}, \text{'communication'}\}$ (8)

The internal events are:

$\delta_{int}(phase, \sigma, inport, wave\_value): S \rightarrow S$

$= (\text{'busy'}, \sigma, p, v)$ if $phase = \text{'communication'}$ and $p \in InPorts$ and $v \in X_p$

$= (\text{'idle'}, \sigma, p, v)$ else.

The external events are:

$\delta_{ext}(phase, \sigma, e, x): Q \times X \rightarrow S$

$= (\text{'idle'}, e, p, v)$ if $phase = \text{'idle'}$ and $p = wave$ and $v = 0 \cdot exp(0)$

$= (\text{'in\_light'}, process\_time, p, v)$ if $phase = \text{'communication'}$ and $p = wave$ and $v = wave\_value \cdot P2Pdefects$

with $Q = \{(s,e) | s \in S, 0 \leq e \leq ta(s)\}$

Output functions are:

$\lambda(phase, \sigma, inport, wave\_value): S \rightarrow Y$

$= (out2, wave\_value \cdot P2Pdefects)$ if $phase = \text{'communication'}$ and $inport = in1$

$= (out1, wave\_value \cdot P2Pdefects)$ if $phase = \text{'communication'}$ and $inport = in2$

State advancing time is:

$ta(\sigma): S \rightarrow \Re^{+}_{0,\infty} = \sigma = bit\_propagation\_time$ (9)

Two states characterize the point-to-point connection behavior, as seen in (8): *idle* (no conversion) and *communication* (light is transported through the optical waveguide). There are 2 internal events: *busy* (light is present), *idle* (no light through the waveguide); and 2 external events: *idle* (no light) and *in_light* (light in one of the inputs). The state advancing time shown in (9) is due to the light transport in a waveguide depending on its length and its manufacture materials. This DEVS description must take into account the attenuation in the point to point connection due to its defects (*P2Pdefects*). These defects attenuate the optical power value at the outputs.

V. Conclusions and Future Work

This paper proposes the formalization of optical-electrical interfaces and basic elements of an optical network on chip using the DEVS approach. This formalization represents an abstraction and generalization of a physical-level solution. Future work includes the verification of opto-electrical interfaces and the definition of a library for automatic generation of opto-electrical interfaces.

Currently, we are creating DEVS models of the opto-electrical interfaces using the CD++ toolkit [10]. CD++ allows the user to create DEVS models, simulate them, and use them in the target platform without modifications Each of the components is being defined as an atomic model in CD++ (for instance, the point-to-point optical connection component is defined as a basic component). Continuous components will be implemented using Quantized States Specifications, and integrated as a multicomponent. This would provide us with an environment for experimentation. Finally, the formal specifications of the DEVS models will be used combined with model checking tools to formally prove timing properties of the application.

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